



PTO/SB/08A (08-03)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1 of 2

Complete if Known

Application Number	10/689,333
Filing Date	October 20, 2003
First Named Inventor	Chen
Art Unit	2827
Examiner Name	
Attorney Docket Number	SAND-01012US0

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
TL		US- 4,627,027	12/2/1986	Rai et al.	—
TL		US- 5,870,334	2/9/1999	Hemink et al.	—
TL		US- 5,949,714	9/7/1999	Hemink et al.	—
TL		US- 6,222,762	4/24/2001	Guterman et al.	—
TL		US- 6,301,151	10/9/2001	Engh et al.	—
TL		US- 6,424,566	7/23/2002	Parker	—
TL		US- 6,522,580	2/18/2003	Chen et al.	—
TL		US- 6,525,964	2/25/2003	Tanaka et al.	—
TL		US- 6,529,412	3/4/2003	Chen et al.	—
TL		US- 20030147278	8/7/2003	Tanaka et al.	—
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FOREIGN PATENT DOCUMENTS

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
TL		Hosono, et al., A High Speed Failure Bit Counter for the Pseudo Pass Scheme (PPS) in Program Operation for Giga Bit NAND Flash, Toshiba Corporation, pp. 23-26.	
TL		Choi, et al., A Novel Booster Plate Technology in High Density NAND Flash Memories for voltage Scaling-down and Zero Progam Disturbance, Samsung electronics Co., LTD., pp. 238	

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